

FIG. 1 (PRIOR ART)

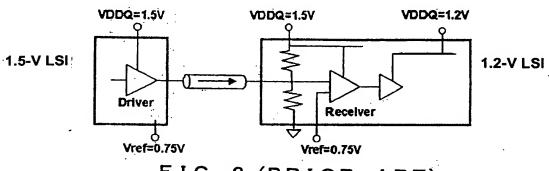


FIG. 2 (PRIOR ART)

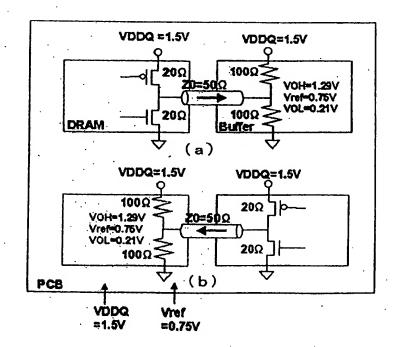


FIG. 3 (PRIOR ART)

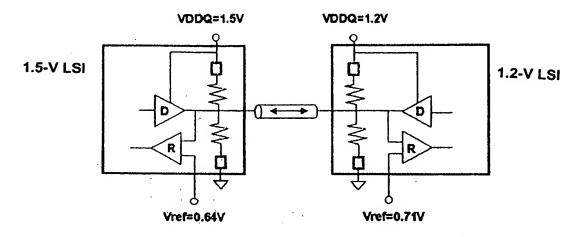


FIG. 4 (PRIOR ART)

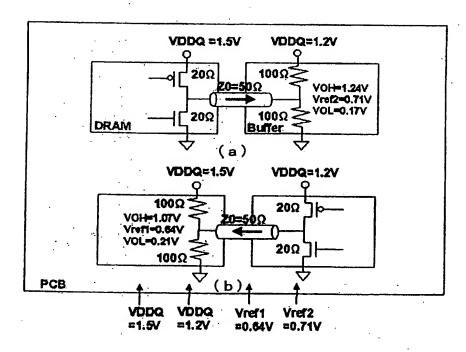


FIG. 5 (PRIOR ART)

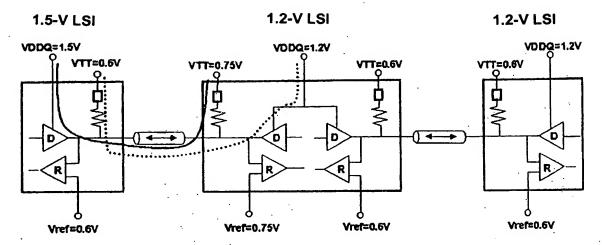


FIG. 6 (PRIOR ART)

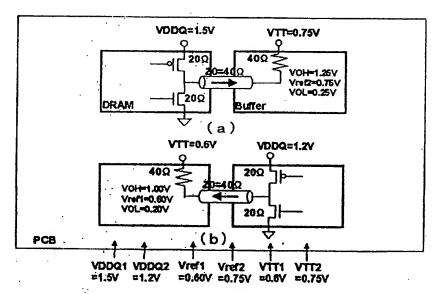


FIG. 7 (PRIOR ART)

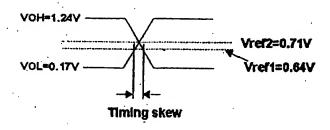


FIG. 8 (PRIOR ART)

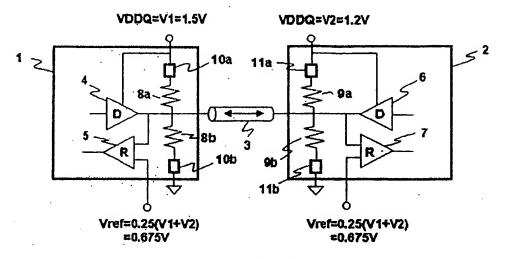


FIG. 9

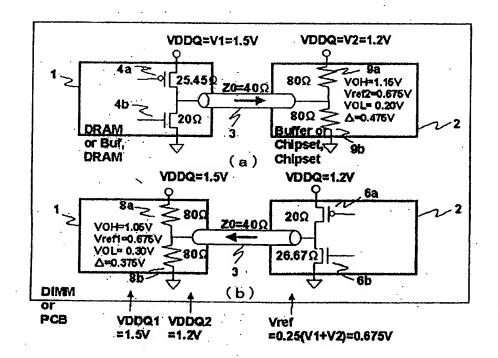
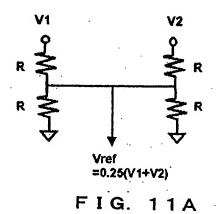


FIG. 10



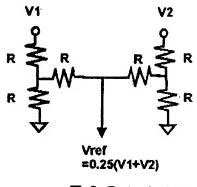


FIG. 11B

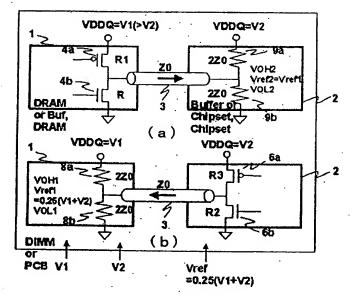


FIG. 12

R ≦ Z0

R1=Z0(V2·Z0-V1·R-V1·Z0) /(V2·R-V1·Z0-V1·R)

VOH2=(V1-0.5V2)Z0/(R1+Z0) + 0.5V2 VOL2=0.5V2-R/(Z0+R)

R3 ≦ Z0

R2=Z0(V1·Z0+V2·R3-V2·Z0) /(V1·R3+V2·Z0-V2·R3)

VOH1=(V2-0.5V1)Z0/(R3+Z0) + 0.5V1 VOL1=0.5V1·R2/(R2+Z0)

Vref=Vref2=0.25(V1+V2)

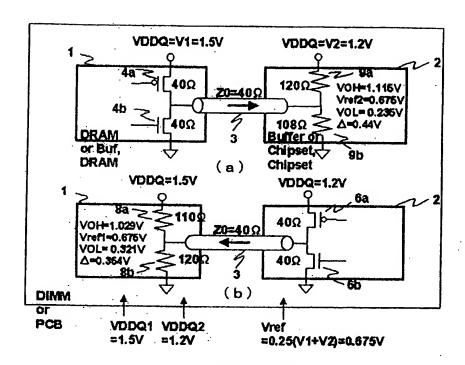


FIG. 13

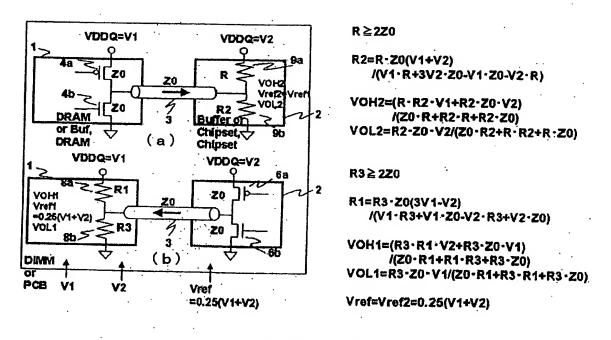


FIG. 14

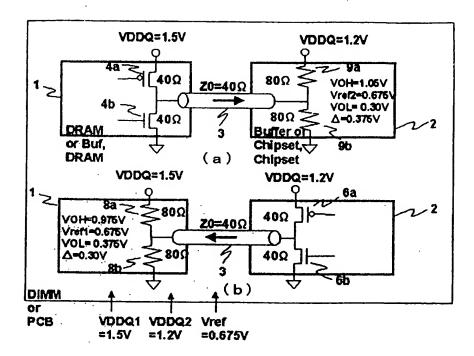


FIG. 15.

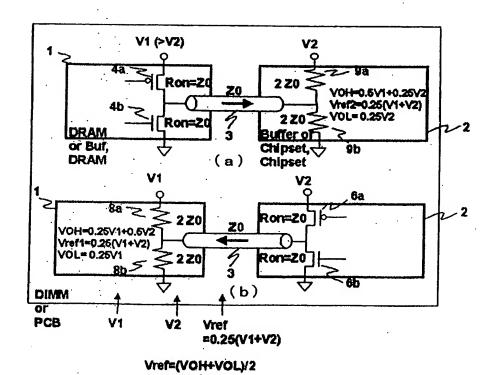
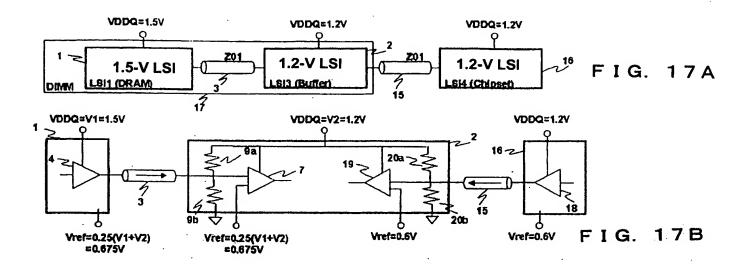
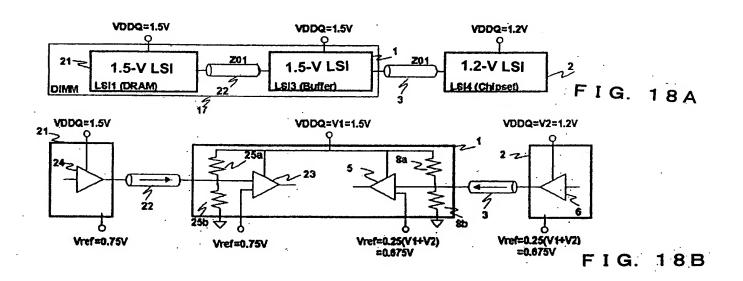


FIG. 16





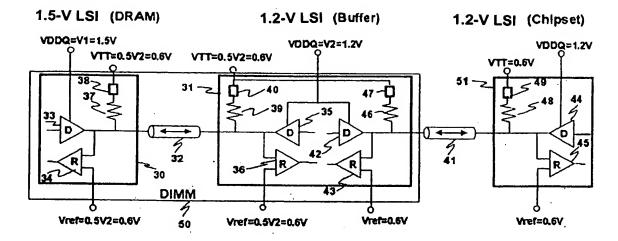


FIG. 19

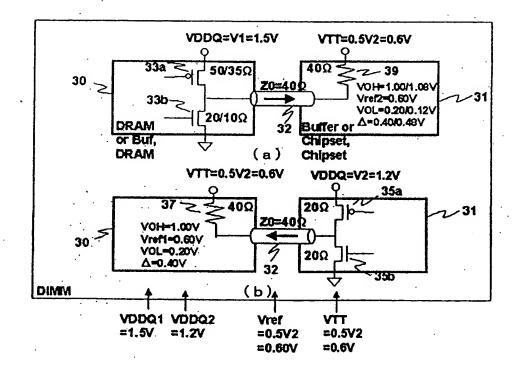
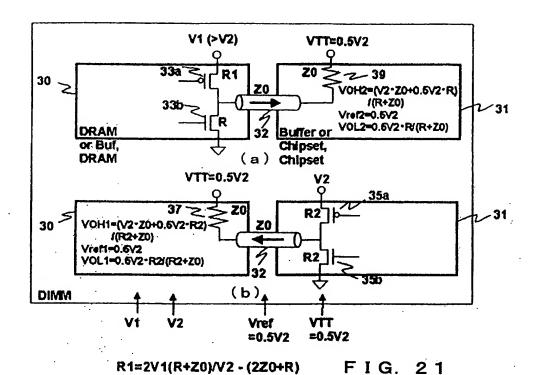


FIG. 20



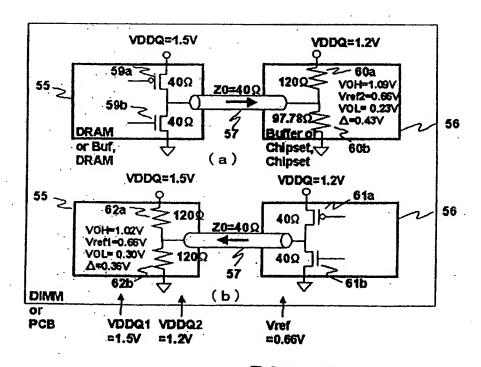
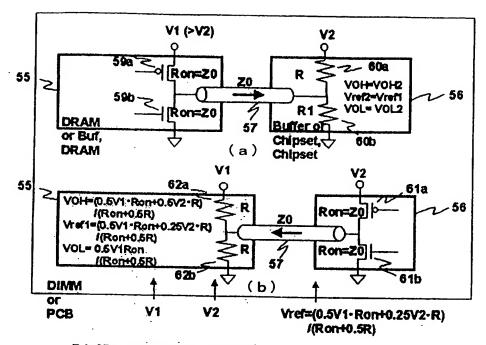


FIG. 22.



R1=2R-Ron(V1-Ron + 0.5V2-R) /(V2-R-Ron + R-R-V1 + 4Ron-Ron-V2-R-R-V2-2Ron-Ron-V1) VOH2=(R-R1-V1+R1-Ron-V2)/(R-R1+R1-Ron+R-Ron) VOL2=R1-Ron-V2/(R-R1+R-Ron+R1-Ron)

FIG. 23

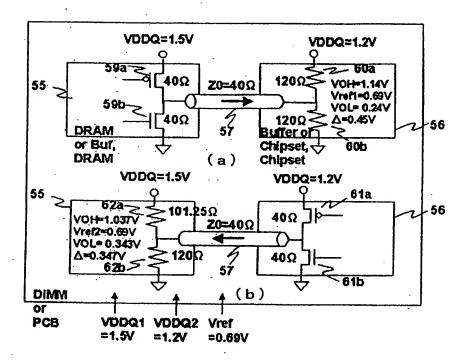
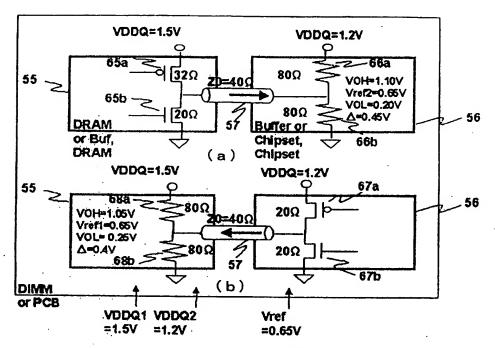
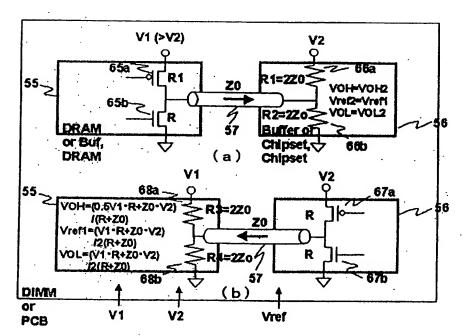


FIG. 24



F.IG. 25



R1=(V1-Z0-Z0-V2-Z0-Z0+0.5V2-Z0-R) /(V1-R+0.5V2-Z0-V2-R) VOH2=(0.5V2-R1+V1-Z0)/(R1+Z0) VOL2=0.5V2-R/(R+Z0)

FIG. 26

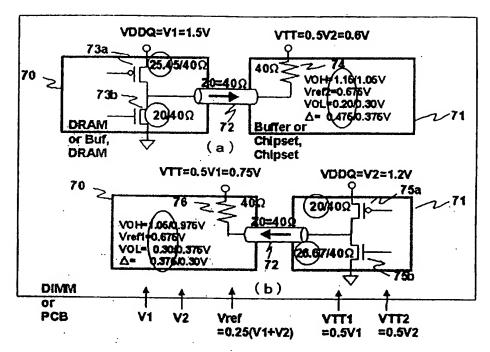


FIG. 27

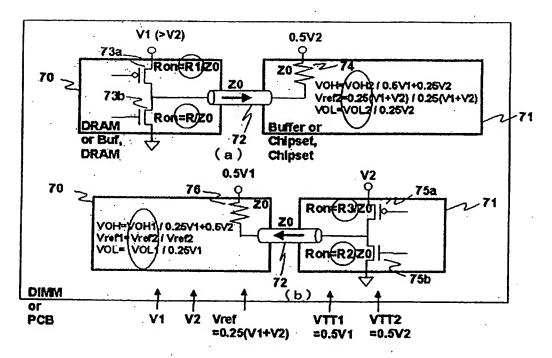


FIG. 28

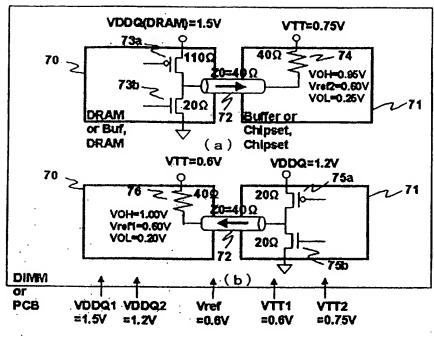


FIG. 29

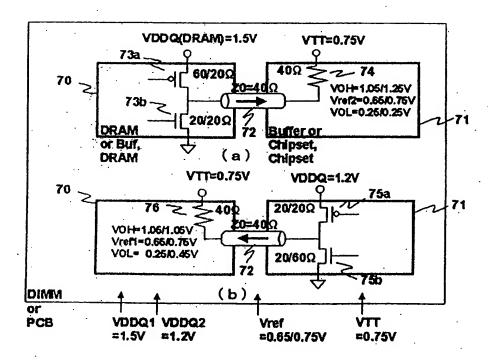
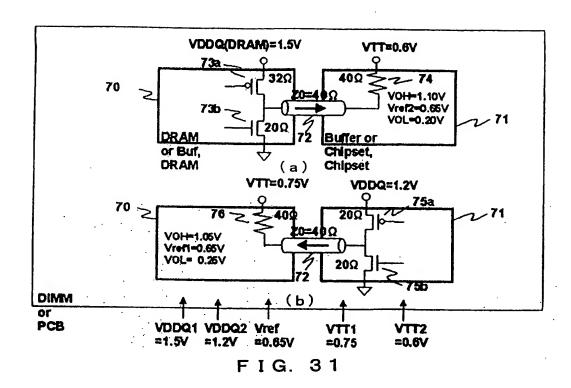


FIG. 30



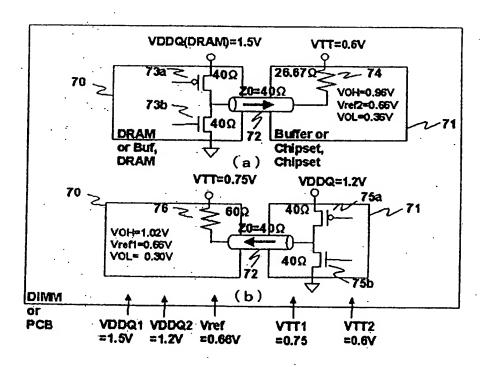


FIG. 32

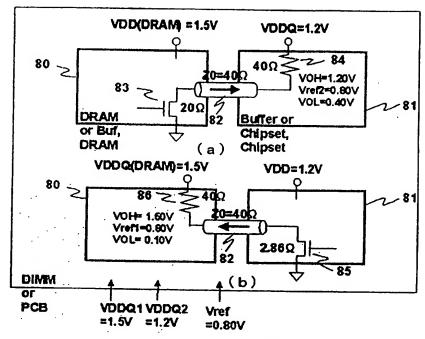


FIG. 33

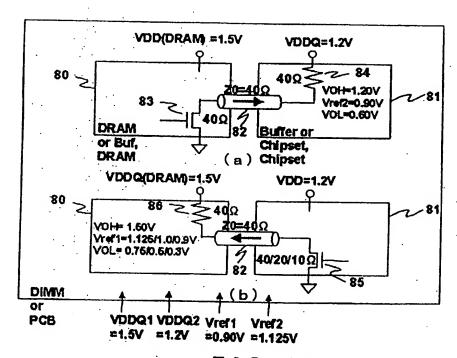
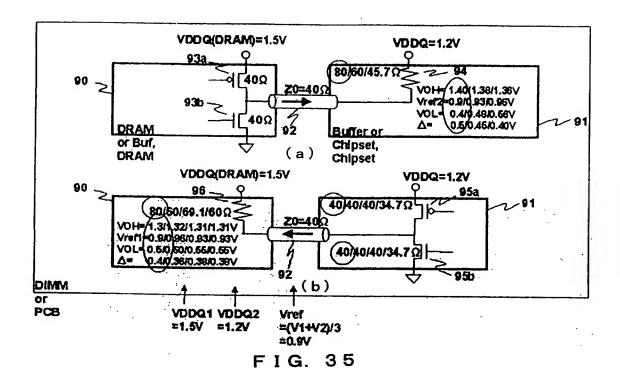


FIG. 34



VDDQ(DRAM)=1.5V VDDQ=1.2V 40Ω VOH= 1.40V Vref2=0.90V 93b VOL= 0.40V Δ= 0.60V 20Ω or Buf, (a) Chipset DRAM VDDQ(DRAM)=1.5V VDDQ=1.2V 20Ω Vref1=0.90V VOL= 0.60V 20Ω **∆=** 0.40∨ 95b DIMM (b) or PCB VDDQ1 VDDQ2 Vref =1.5V =1.2V =(V1+V2)/3 =0.9V

FIG. 36

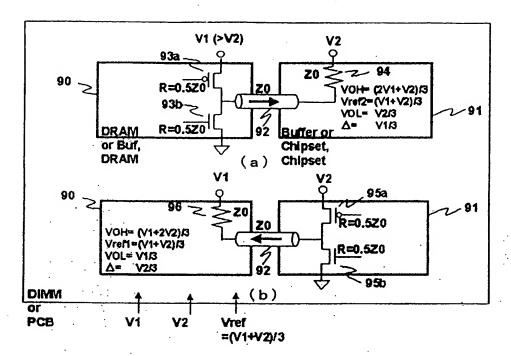


FIG. 37

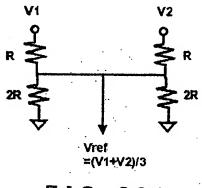


FIG. 38A

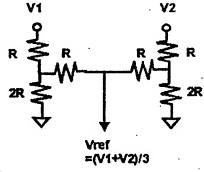
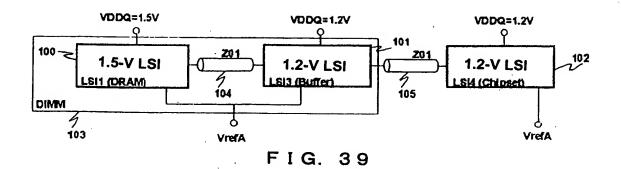


FIG. 38B



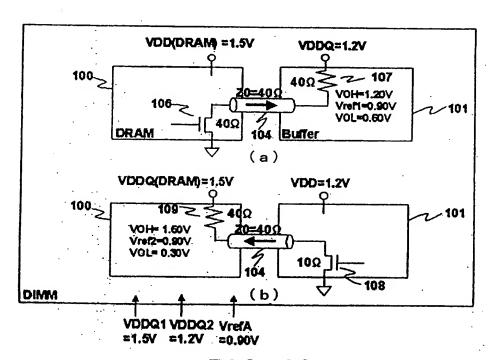


FIG. 40

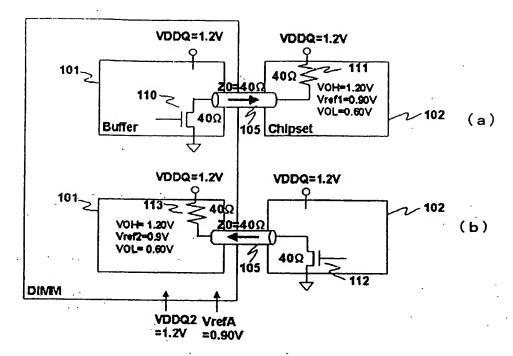


FIG. 41

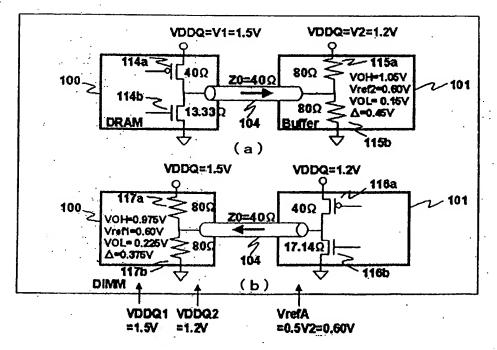


FIG. 42

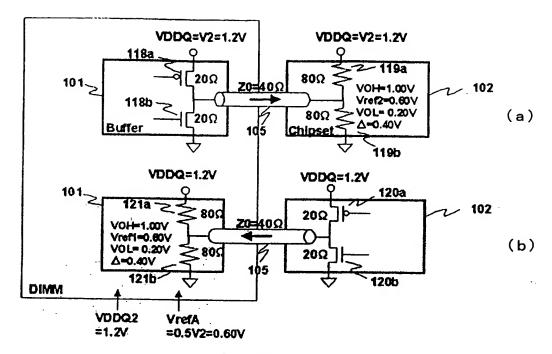


FIG. 43

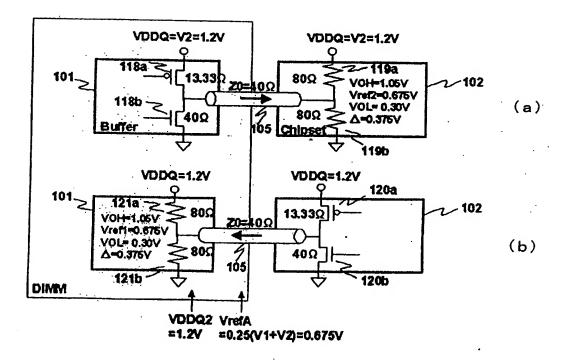


FIG. 44

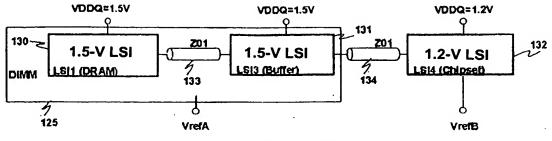


FIG. 45

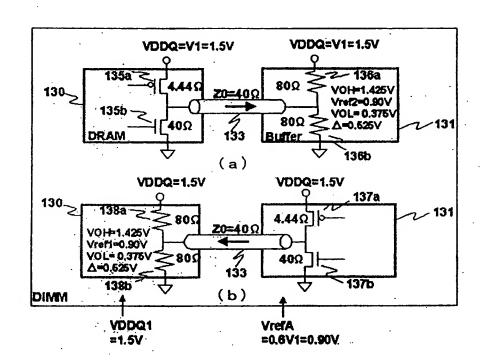


FIG. 46

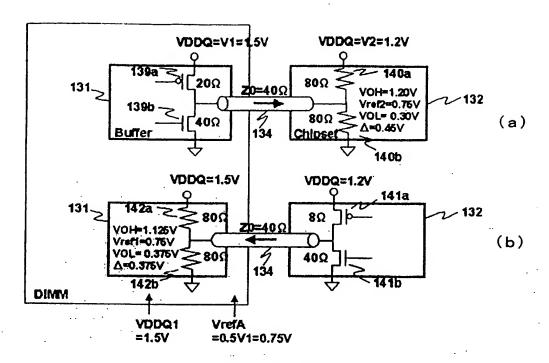


FIG. 47

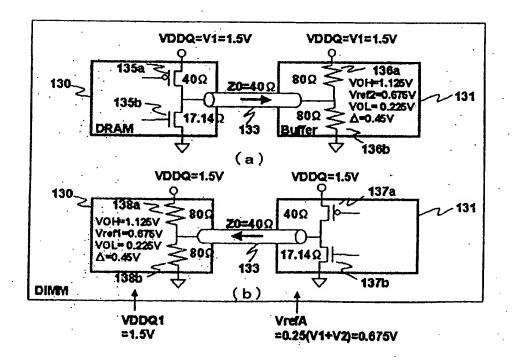
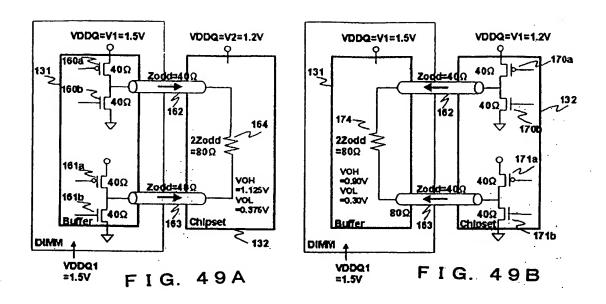
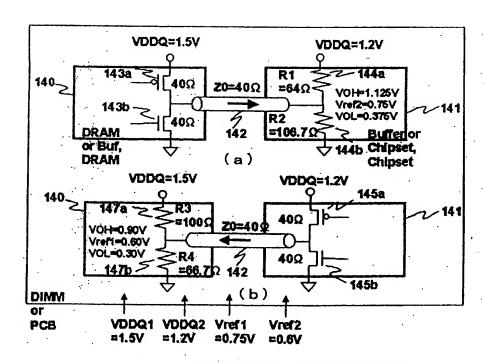


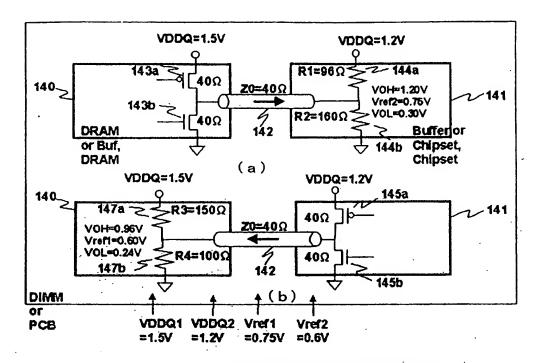
FIG. 48





m=(R1//R2)/Z0=s=(R3//R4)/Z0=1.0

FIG. 50



m=(R1//R2)/Z0=s=(R3//R4)/Z0=1.5

FIG. 51

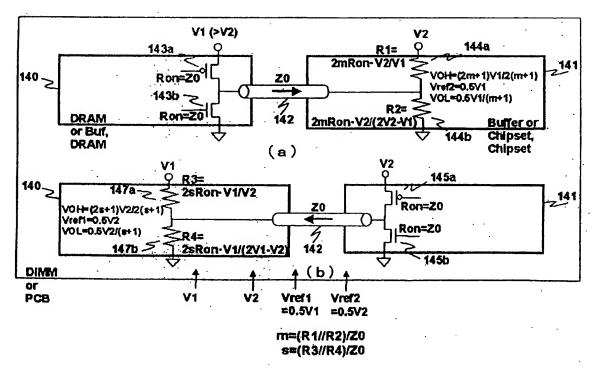
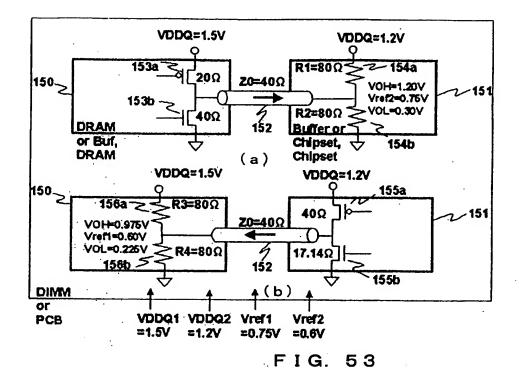


FIG. 52



V1 (>V2) **V2** 153a Q Ron1= 150~ 2-154a 0.25V2-Z0 R1=2Z0 VOH=(0.6V2 · Ron1+V1 · Z0) I(V1-0.75V2) ZO I(Ron1+20) 153b Vref2=0.6V1 VOL-0.25V2 R2=2Z0 Ron=Z0 DRAM Buffer or or Buf, Chipset, 154b DRAM Chipset (a) V1 155a 156a ~ R3=2Z0 151 Ron=ZQ VOH=0.25V1+0.5V2 Vref1=0.5V2 ZO VOL=0.5V1-Ron4 CR4=220 Ron4= /(Ron4+Z0) Z0/2V2-V1) 1(3V1-2V2) 156b DIMM (b) OF PCB V1 V2 Vref1 Vref2 =0.5V1 =0.5V2

FIG. 54